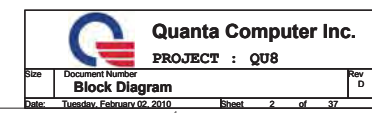



Model	REV 1B	CHANGE LIST						MODEL		
								FROM		To
MB		A (ET1 to ET2) stage :REV:C						1		1C
		1.11/12 P8---add R566,R567 for DMI CLK FUNCTION						2		1C
		2.11/12 P8---add R176,DEL R174 for CLK frequency						3		1C
		3.11/12 P7---add R416,DEL R46 for CFG STRAP						4		1C
		4.11/23 P13---change KBSMI# PIN (GPIO9)						5		1C
		5.11/22 P14---add R181,R187 for PCH_TRST_N pin,del R464						6		1C
		6.11/23 P14---modify SMBUS function						7		1C
		7.11/24 P15---change display port pin net						8		1C
		8.11/12 P15---del PCH DMI CLK						9		1C
		9.11/12 P16---change PCH GPIO pin(del R244,R581,add R211)						10		1C
		10.11/23 P17---del R452, add R455 for disable AT-D function)						11		1C
		11.11/23 P17---change BIOS from +P3V3_S5 to +VCC3_ME						12		1C
		12.11/25 P17---change ME power from +P3V3_+VCC3_ALWAYS						13		1C
		13.11/23 P21---modify EDID switch function						14		1C
		14.11/23 P21---add 3 X 1 pin header for EDID						15		1C
		15.11/23 P22---change TPM IC from WPCIT210 to ST19NP18						16		1C
		16.11/24 P23---add F5,DEL F4 (change webcam power)						17		1C
		17.11/24 P25---change U14 (footprint error)						18		1C
		18.11/22 P25---add J4(HDD POWER)						19		1C
		19.11/24 P26---change Right board.back board connector						20		1C
		20.11/22 P27---del D14,D14,R346.(power sequence issue)						21		1C
		21.11/22 P27---change PS2 power from +P5V_S5 to +P5V_always						22		1C
		22.11/22 P27---add MMB board power						23		1C
		23.11/24 P27---modify EC SMBUS issue						24		1C
		24.11/12 P28---DEL PQ19,PQ56,PQ56(power on issue)						25		1C
		25.11/22 P31---change PQ40,PQ35(for control +PSV_USB_S3,+PSV_DDR_S3 power)						26		1C
		26.11/22 P33---add main control +VCC1_8 PCH_S0						27		1C
		27.11/22 P35---add main control +CPU_VTT_S0						28		1C
		B (ET2 to SDV) stage :REV:D						29		1C
		1.12/10 P7---add Co-lay Thermal IC.						30		1C
		2.12/10 P14---change R247,R524,R1138,R540,R522 to 0 ohm for audio function						31		1C
		3.12/10 P14---add Q70,Q71 2n7002,N/A RS89,RS90 for SMBUS						32		1C
		4.12/10 P15---add C392,C393 0.1uF(modify DDP_C_AUX)						33		1C
		5.12/10 P15---DEL R146,R150(N/A DPCCLK_PCH,no output clock.)						34		1C
		6.12/10 P21---N/A D3(del VGA IN power)						35		1C
		7.12/10 P21---Add signal 2270_FUN6,7# and pull hi V33P_VGAIN for OSD function						36		1C
		8.12/10 P23---Add common choke at Web CAM module						37		1C
		9.12/10 P23---R9,R10 change to 220ohm for webcam EMI						38		1C
		10.12/10 P23---modify BT enable power +P5V_S0						39		1C
		11.12/11 P24---remove CBP/CBN AGND						40		1C
		12.12/10 P24---remove Cap,add R20,R21,R22,R25 at speaker.						41		1C
		13.12/10 P24---add I3.2,I.33 Bead(add power bead for audio percision)						42		1C
		14.12/10 P24---Change PVDD1/PVSS/PVDD2 from DGND to AGND						43		1C
		15.12/10 P26---modify right io board connect pin7 and pin8 to GND						44		1C
		16.12/10 P27---Change EC and Scalar GPIO define						45		1C
		17.12/10 P27---change Power rail from P5V_S0 to P5V_always for PIR issue						46		1C
		18.12/11 P28---add PC277,PC278,PC276 for modify signal sequence.						47		1C
		19.12/11 P28---change Q39,Q40 to BA001440013						48		1C
		20.12/11 P31---modify PQ12,PQ36,Q15,Q16,Q26,Q68 for sometime can't boot issue						49		1C
		21.12/11 P31---PR112,PR114 Chane power rail from P5V_S0 to P5V_always for S3 issue						50		1C
		22.12/11 P30---Add PC275_PC68 220uF/9m Ohm change to 330uF/6m Ohm for VTT transient						51		1C
		23.12/11 P34---Add PC274 for VAXG Vin						52		1C
		24.12/11 P33---add PC271 for +PIPO5V_ME Vout ripple						53		1C
		25.12/11 P31---mount PC4,PC7 for +P5V_S0 and +P3V3_S0 input Voltage						54		1C
		26.12/11 P30---mount PC49 for +DDR1V5_S3 input Voltage						55		1C
		27.12/10 P31---change PQ43(NTMS4800N),PQ44(NTMS4873)						56		1C
		to NTMFS4921NT1G for +P5V_S0 Iout current								
		C:REV:E								
		1.12/23 P14-del R116,R535;add R118,R514 for CMOS function								
		2.12/23 P21-U8 pin 7 pull gnd								
		3.12/23 P21-U6 pin 61 change 2270_fun4#-for OSD function								
		4.12/23 P21-U6 pin 56 change PWM3 -for OSD function								
		5.12/23 P26---Change Right IO CONNN pin8 from GND to +P3V3_S0, pin7 from GND to KC								
		6.12/23 P21---add SW_CRT1 function-for vga monitor								
		7.12/29 P21---Change R615 from 100K 6 to 1K 6								
		8.12/28 P26---Change CN37 Pin2 from VGA_5V To +VCC1_8_PCH_S0								
		9.12/28 P27--- U16 pin 97 change S3_N-for S3 issue								
		PROJECT MODEL :								
		PART NUMBER:								
		APPROVED BY: Alan Chuang #15569								
		DATE:								
		DOC NO:								
		REVISION: IC								
		SHEET								
		1 OF 1								

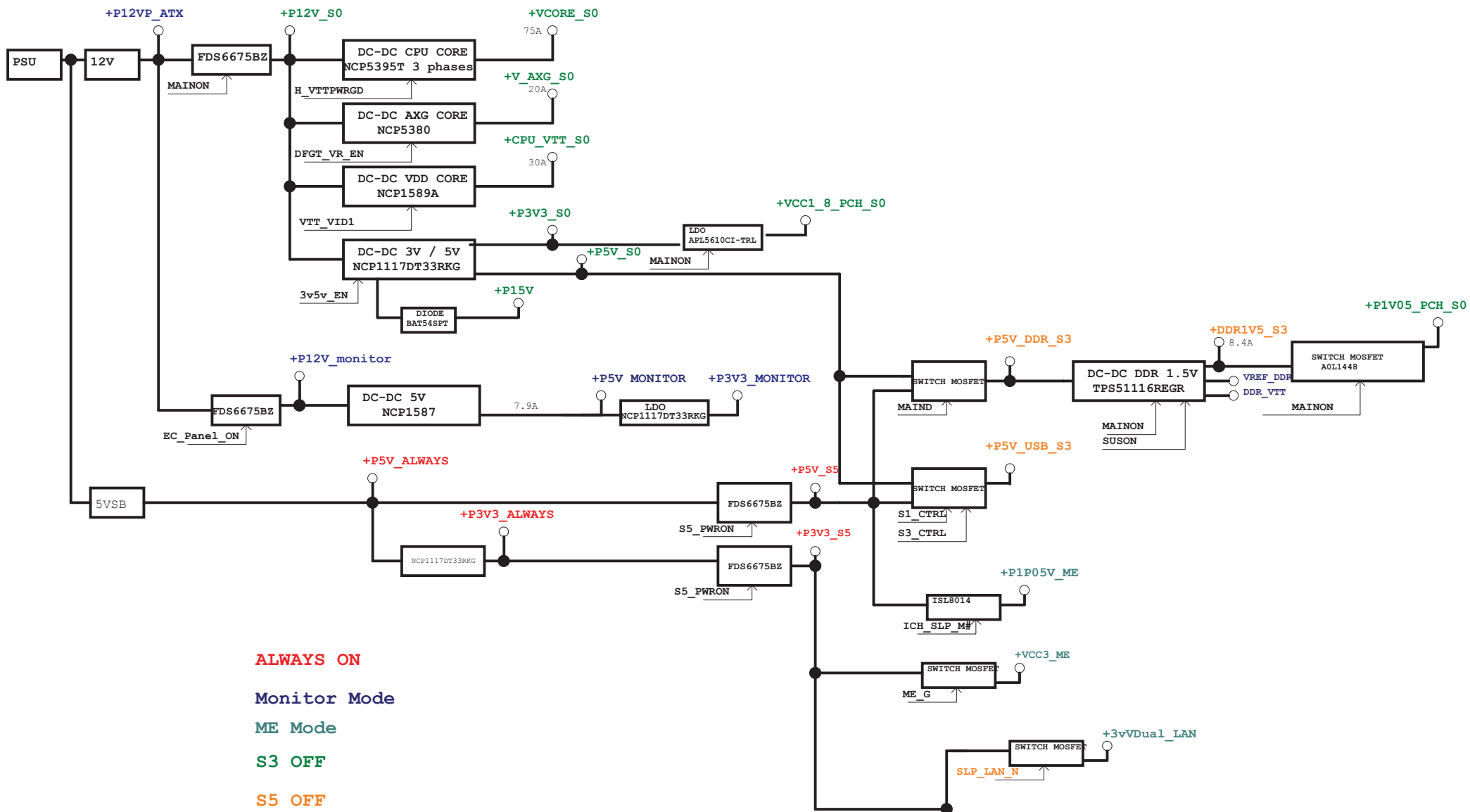
WWW.AliSaler.Com



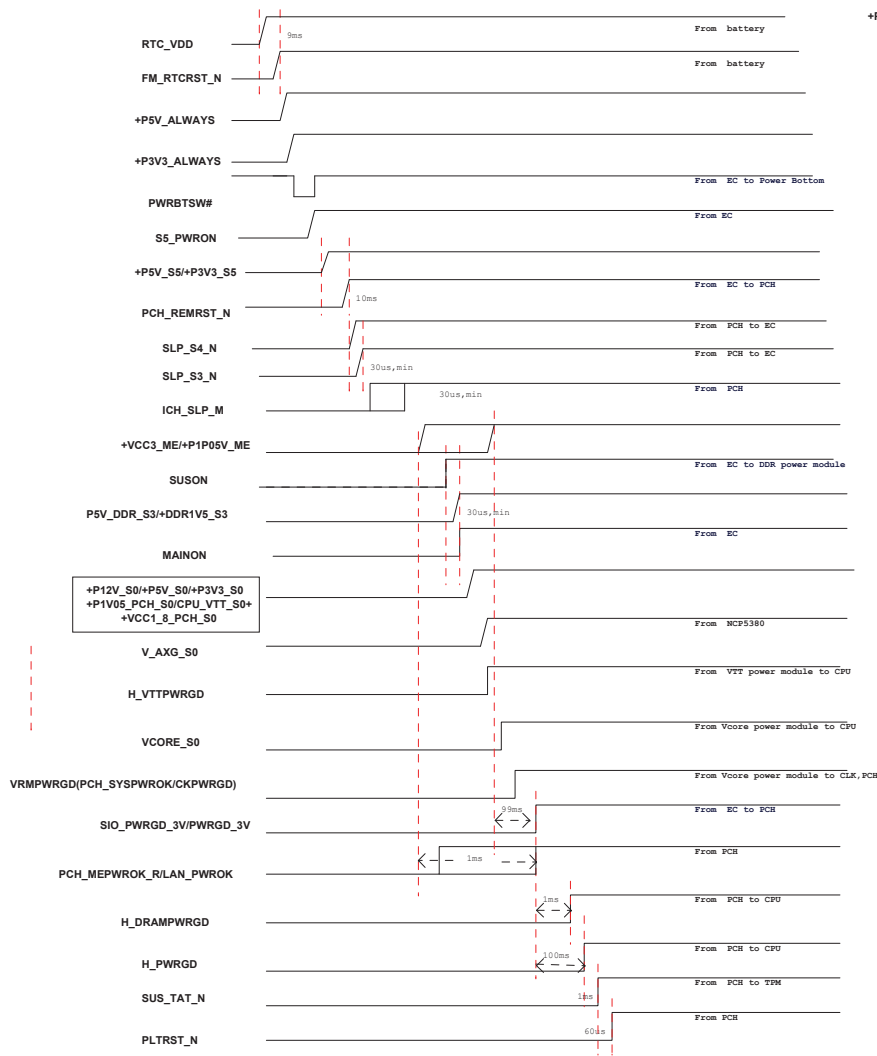
Schematic Page Description :

01-CHANGE LIST	21-SCALAR RTD 2280
02-Block Diagram	22-MINI CARD / TPM
03-Page Description	23-WEBCAM/TOUCH
04-Power Map	24-AUDIO CODEC ALC269
05-Power Sequence	25-SATA/Asset ID
06-CK505_B CLOCK GENERATOR	26-Daughter Board
07-MCP-CLK,CTRL,MISC/THERNAL	27-EC-ITE8512N/FAN CN
08-MCP - PCIE, DMI	28-PSU/+P5V_S5/P3V3_S5
09-MCP - DDR3 CHANNEL A.B	29-CPU_CORE (NCP5395T)
10-MCP - VCCP CONNECTIONS	30-DDR3/VTT1.5V(TPS51116REGR)
11-MCP - MISC VCC & GND	31-P3V3/P5V PC/+P5V_USBS3/DDRS3
12-DDR3-CHA.B-DIMM1A.1B	32-P3V3/P5V MONITOR
13-PCH-DMI, PCI-E, USB.PCI	33-P1V8/P1V05/P1V05_ME/P1V5
14-PCH-PM, GPIO, SMB, RTC, HDA	34-VAXG (NCP5380A)
15-PCH-DISPLAY , FDILINK.CLOCK	35-CPU_VTT(NCP1589A)
16-PCH-SATA	36-SCREW HOLD, M/E
17-PCH-NV RAM (ONFI)/N FLASH	37-GPIO List
18-PCH-POWER	
19-PCH-GND	
20-LCDPANEL /Inverter	

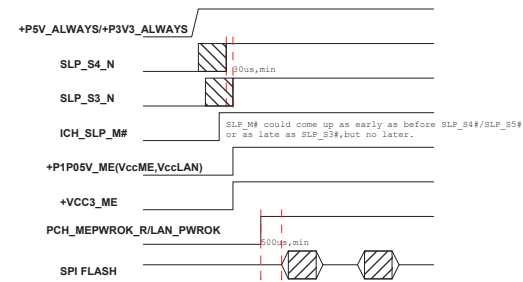
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		PROJECT : QU8	
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Page Description			
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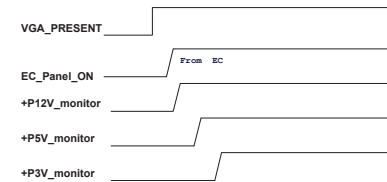
power on Sequence



SLP_M#, M3 ON

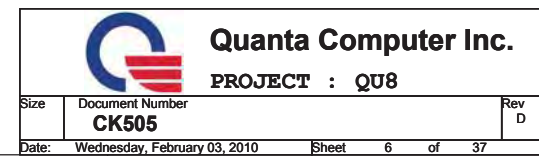


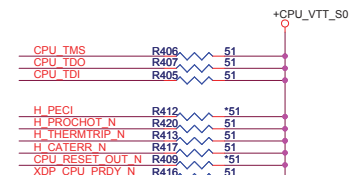
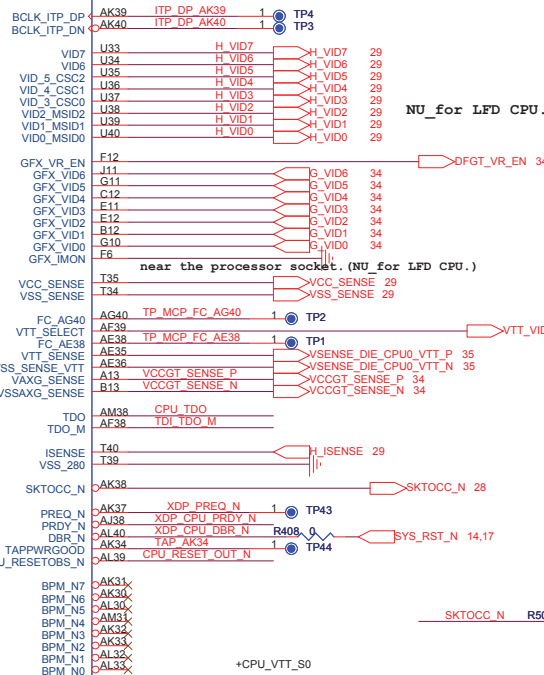
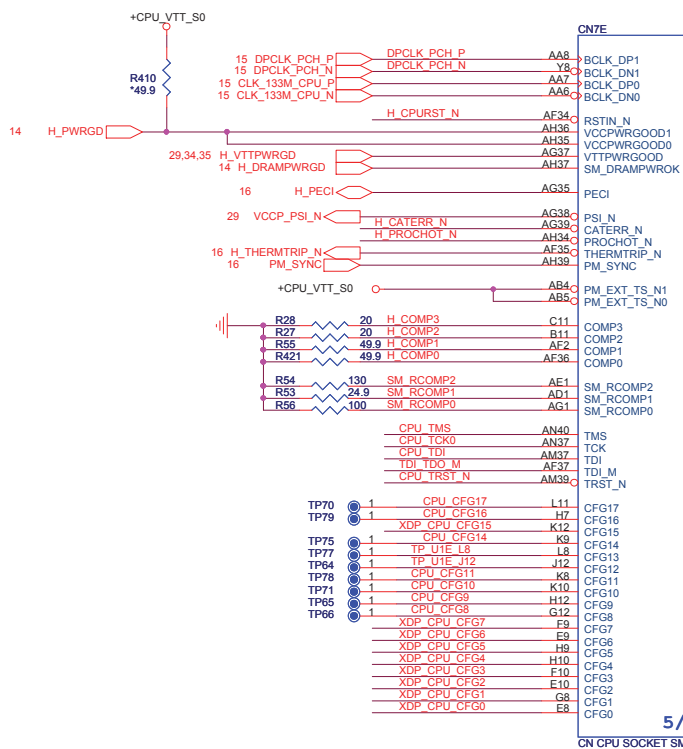
VGA_IN



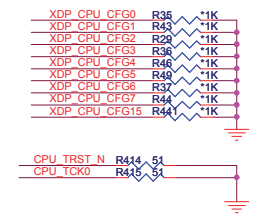
Voltage Rails

Power	Voltage	S0-S2	S3	S4	S5	Cti Signal
+P5V_ALWAYS	5V	V	V	V	V	
+P3V3_ALWAYS	3.3V	V	V	V	V	
+P5V_S5	5V	V	V	V	V	S5_PWRON
+P3V3_S5	3.3V	V	V			S5_PWRON
+VCC3_ME	3V	V	V			ME G
+P1P05V_ME	1.65V	V	V			ICH SLP M
P5V_DDR_S3	5V	V				BUS0/MAINON
+DDR1V5_S3	1.5V	V				BUS0/MAINON
+P12V_S0	12V	V				MAINON
+P5V_S0	5V	V				MAINON
+P3V3_S0	3.3V	V				MAINON
+VCC1_8_PCH_S0	1.8V	V				MAINON
P15V	1.5V	V				MAINON
+P1V05_PCH_S0	1.65V	V				MAINON
CPU_VTT_S0+	1.1V	V				MAINON
V_AXG_S0	1.1	V				CPU_VTT_S0+
VCORE_S0	1.1	V				H_VTTPWRGD
+P12V_monitor	12V	V				EC_Panel_ON
+P5V_monitor	5V	V				EC_Panel_ON
+P3V_monitor	3V	V				EC_Panel_ON





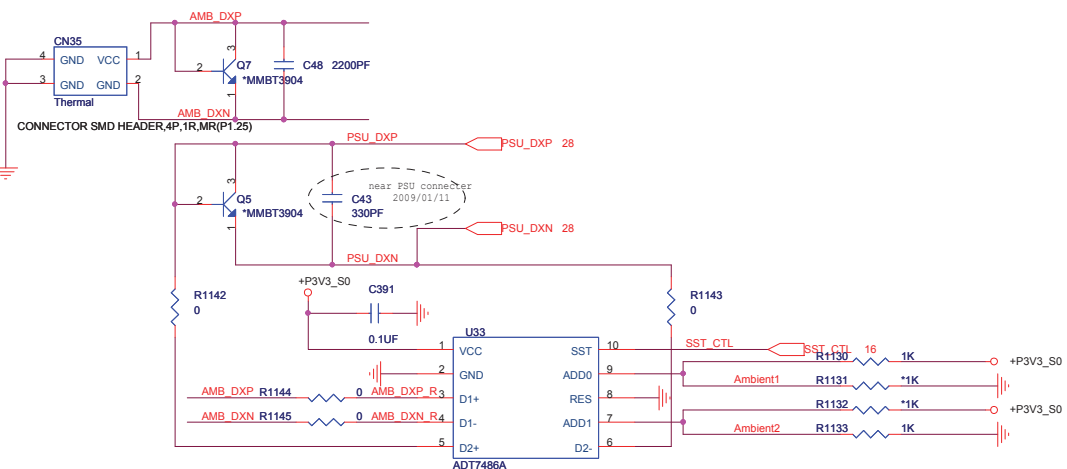
DESIGN NOTE: ENG FEATURE: CFG STRAPS



CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

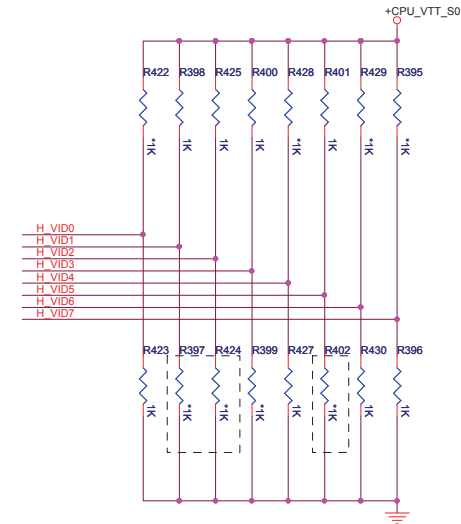
CFG	H	L	Notes
0			
1	RSVD		H:1x16, L:2x8
2	RSVD		
3	NORM	RSVD	LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		

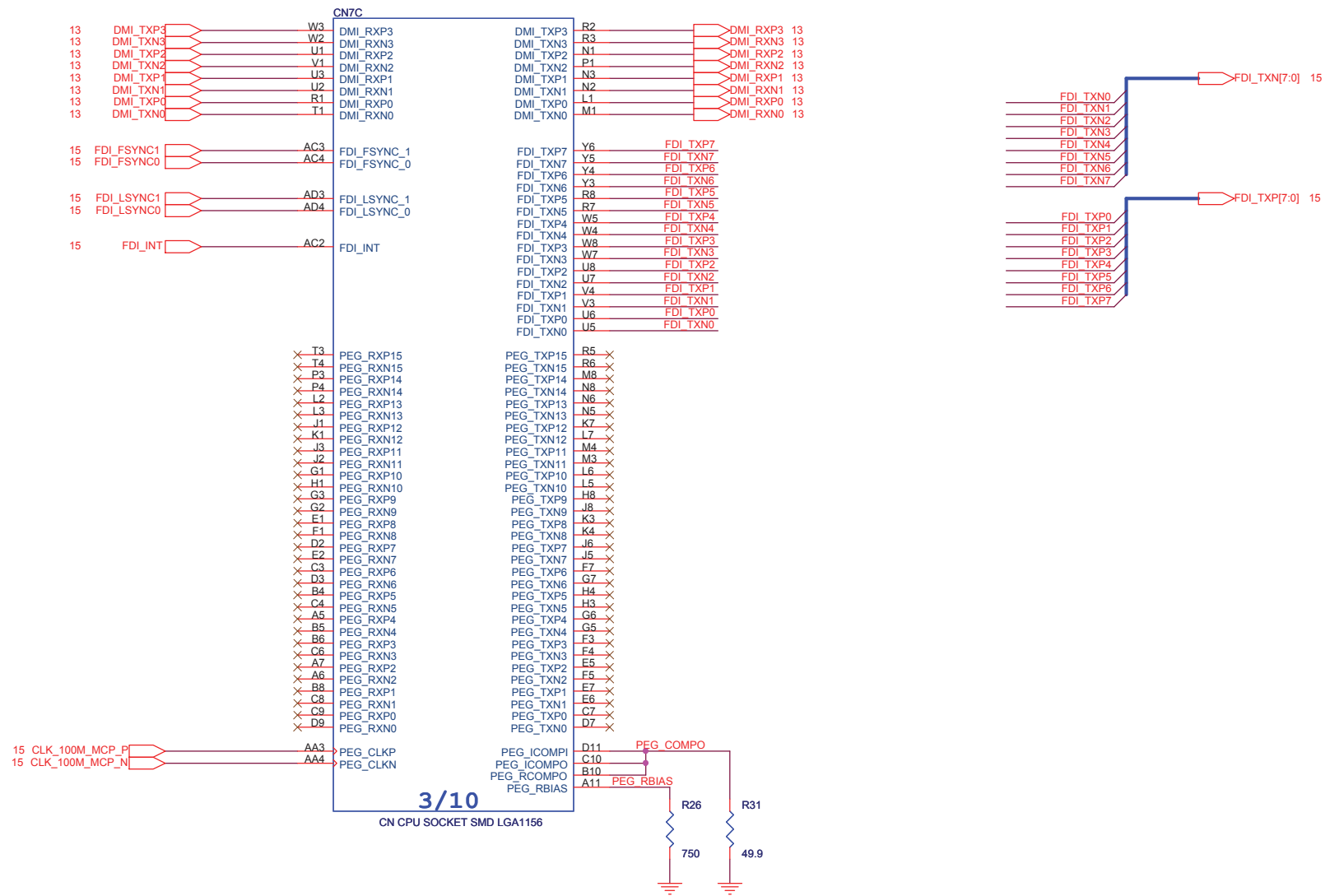
CPU / Ambient / PSU THERMAL SENSOR



<check list>
Layout Note: Routing 10:10 mils and away from noise source with ground guard

Need to be placed close to processor to minimize ESD risk

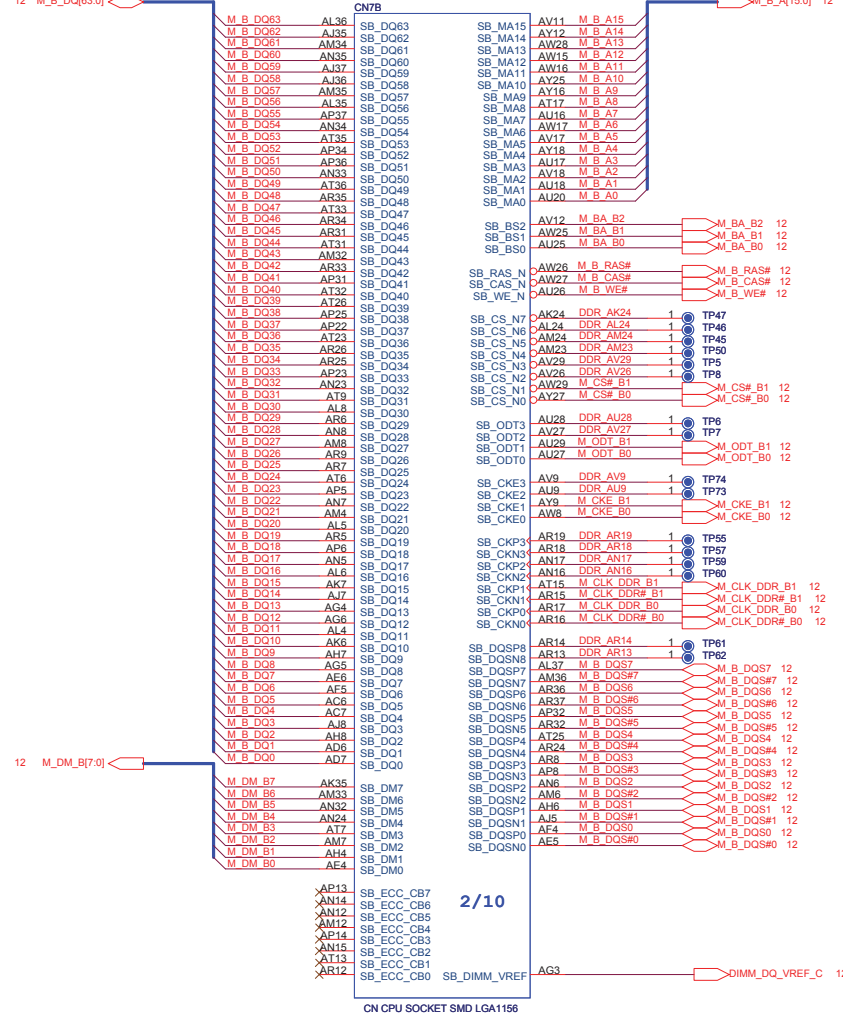
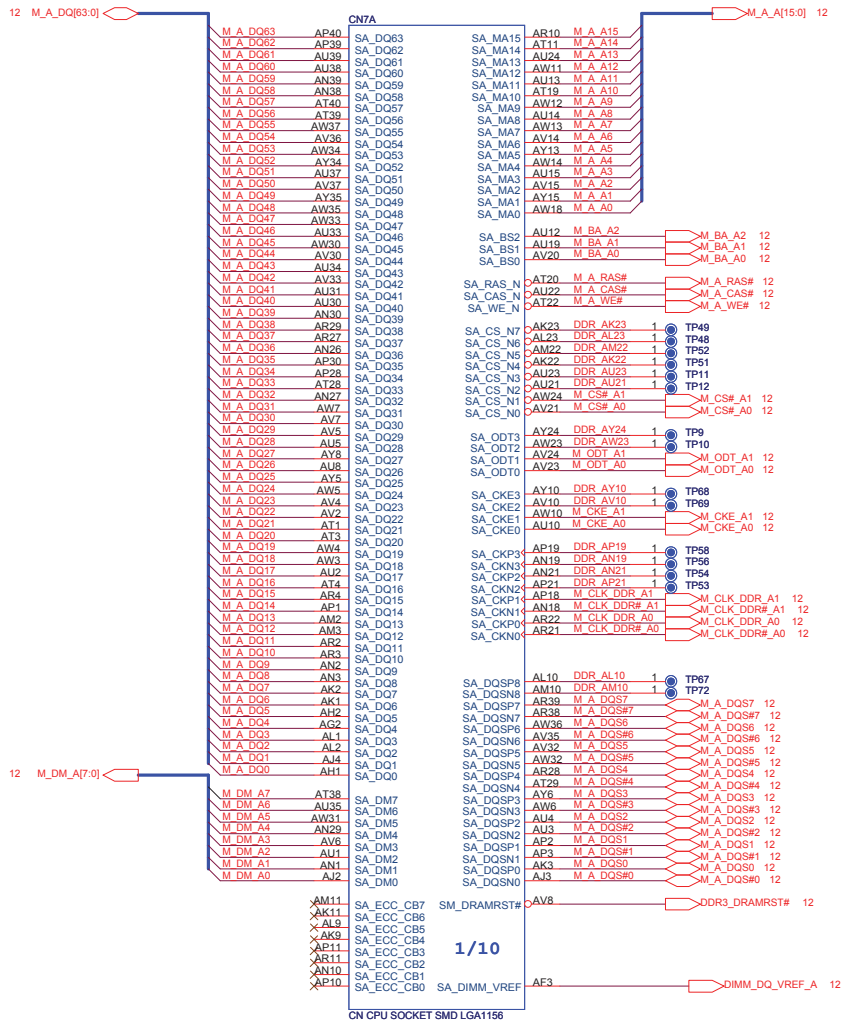


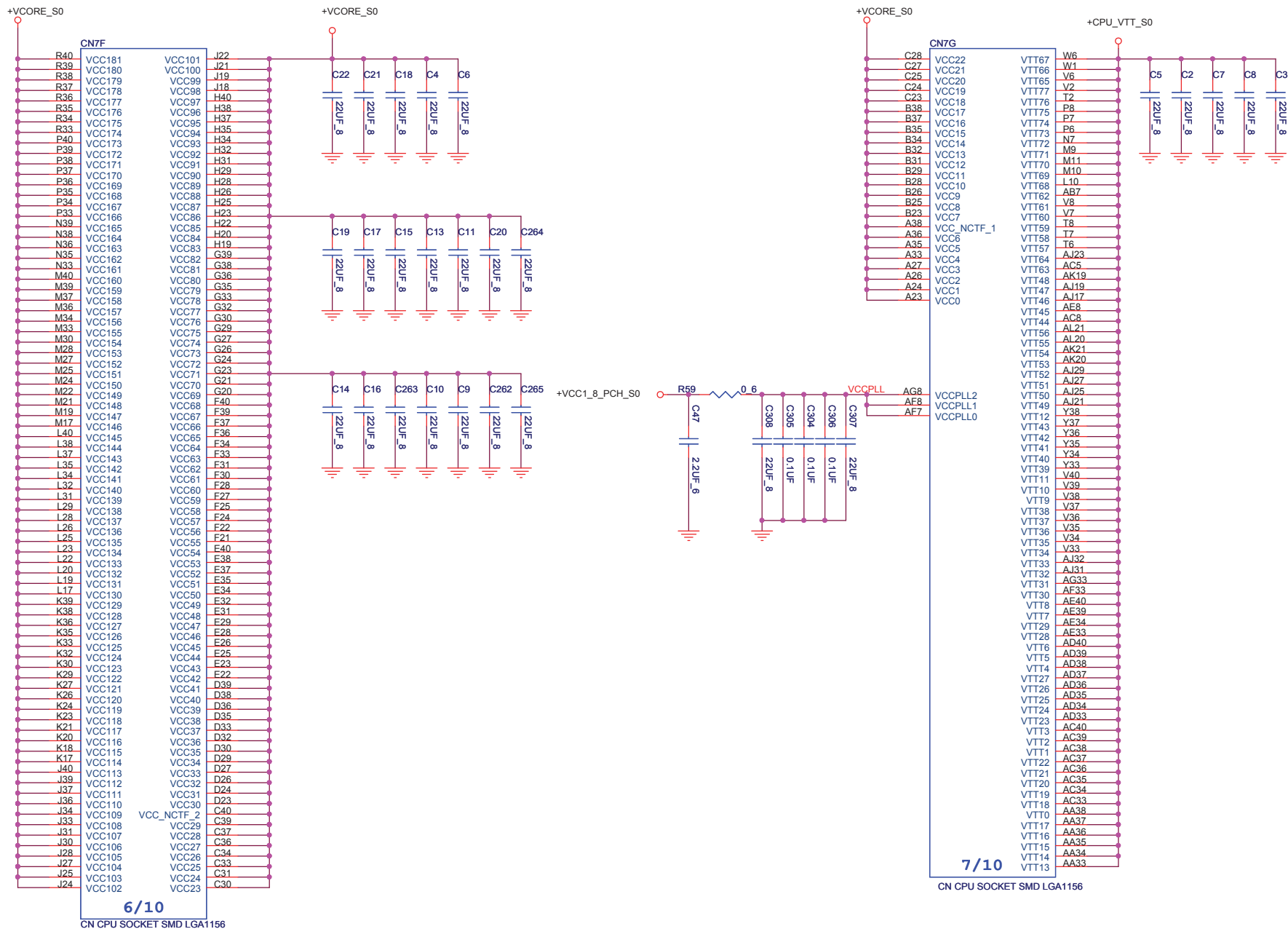


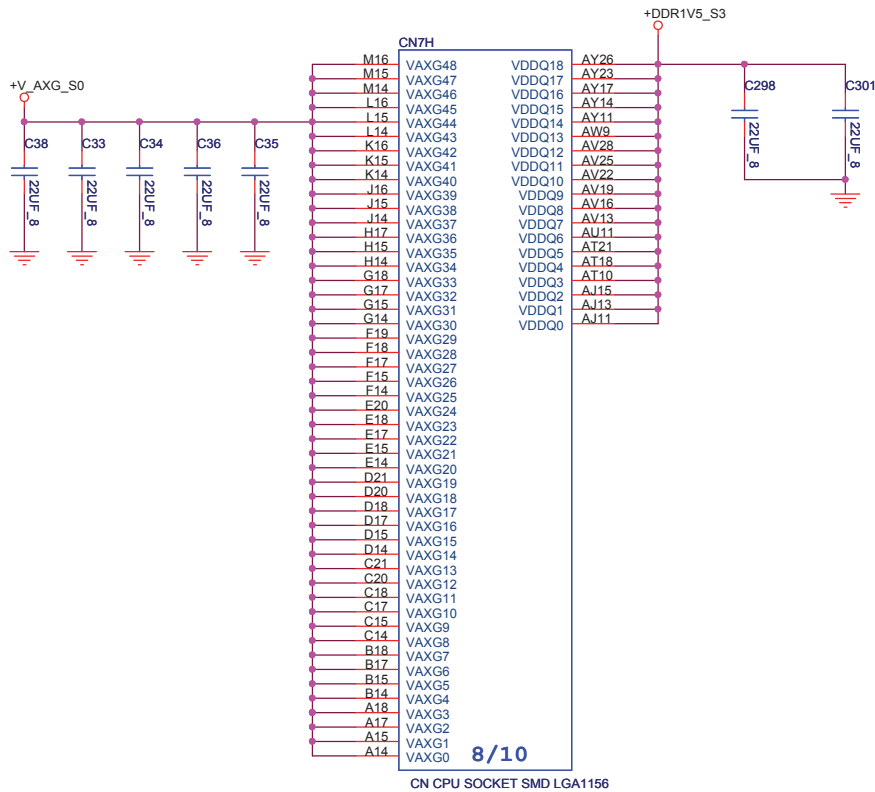
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	MCP-PCIE/DMI	D
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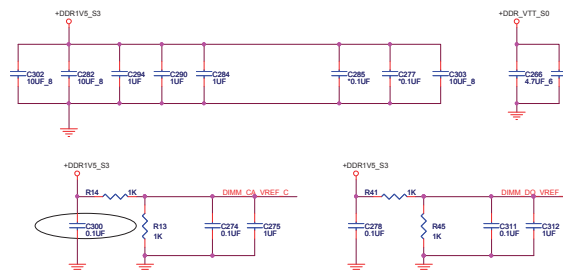
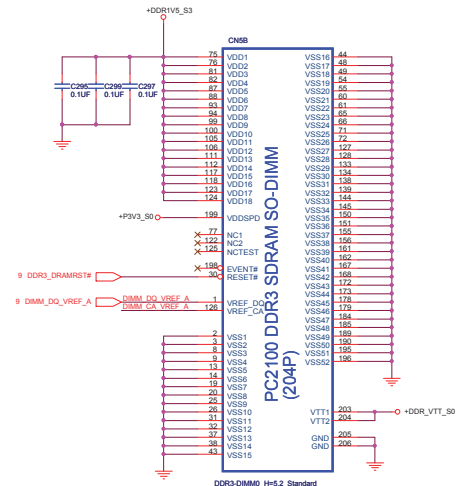


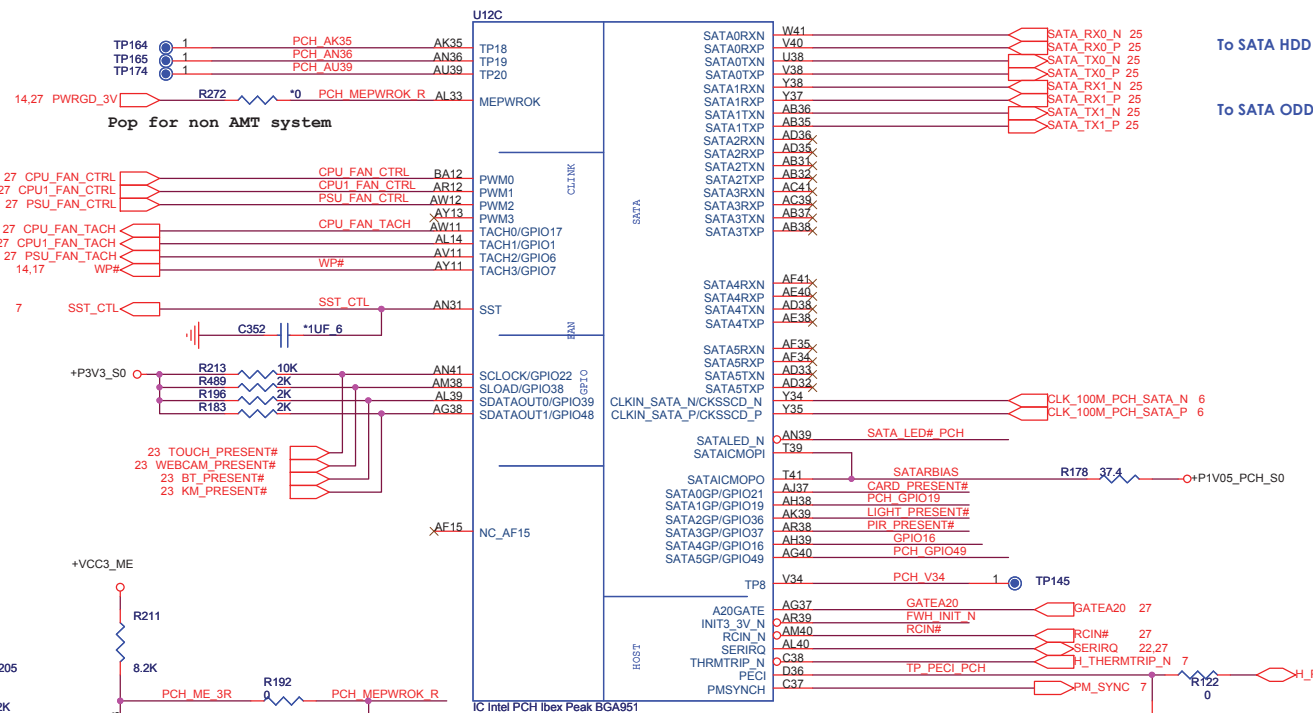


9 M_A_DQS[7..0] 9 M_BA_A[0..2]

9 M_A_DQ[0..63] 9 M_DM_A[7..0]

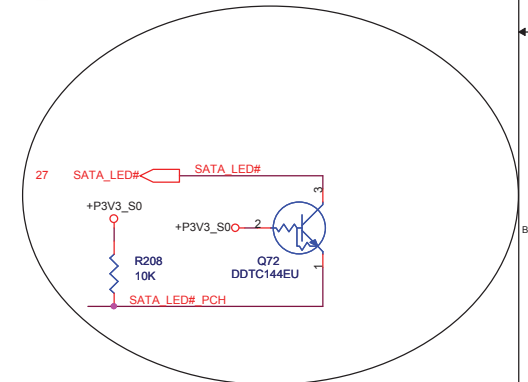
9 M_A_A[15..0] 9 M_A_DQS#[7..0]

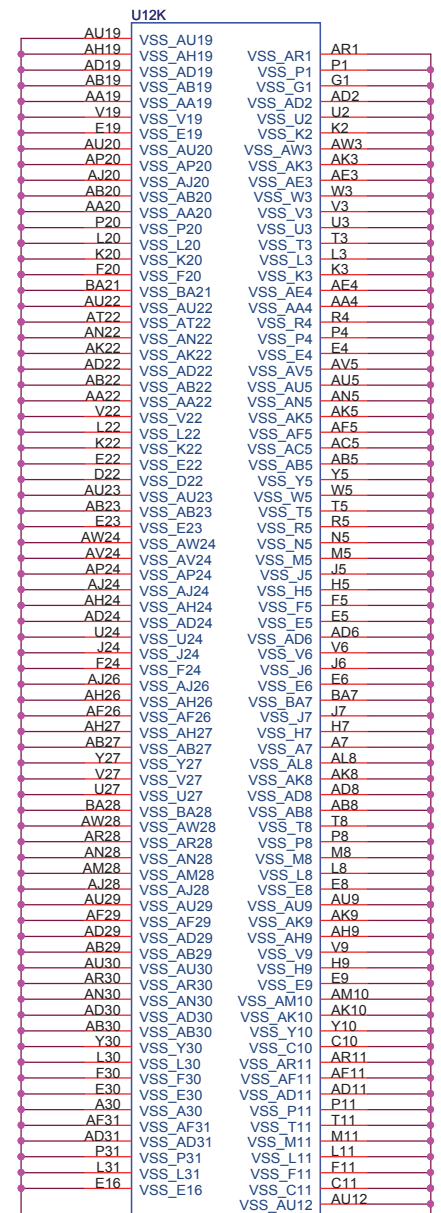




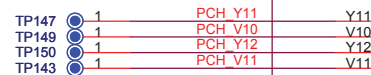
To SATA HDD

To SATA ODD



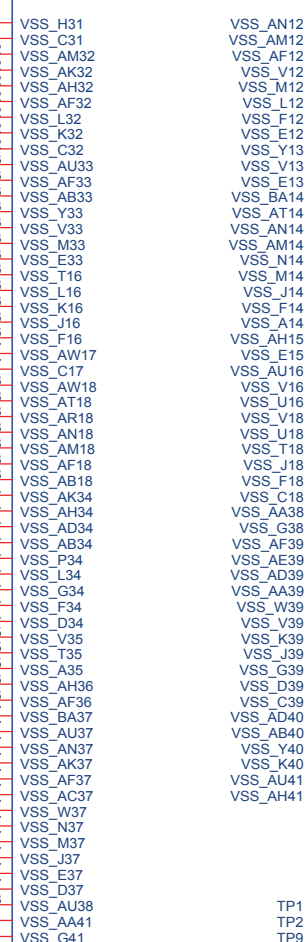


IC Intel PCH Ibex Peak BGA951

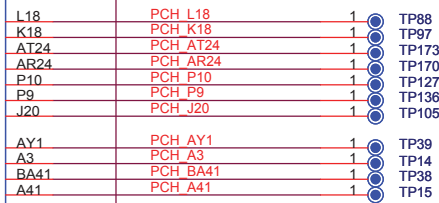
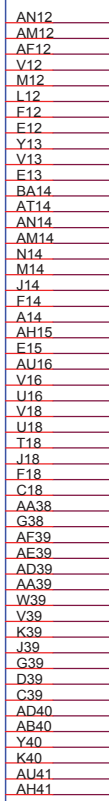


IC Intel PCH Ibex Peak BGA951

U12L



TP21



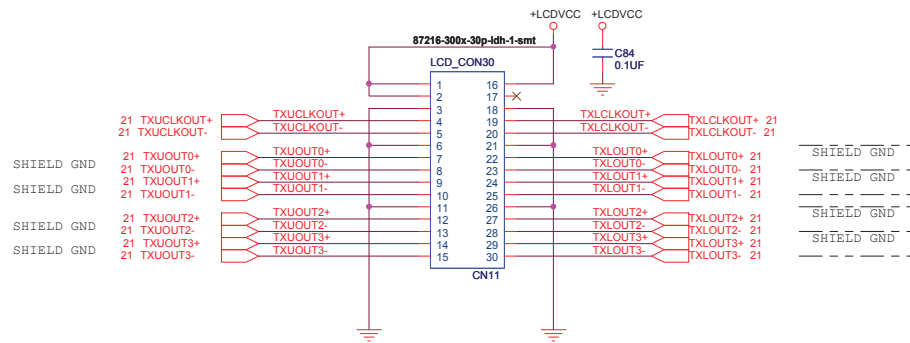
TP163



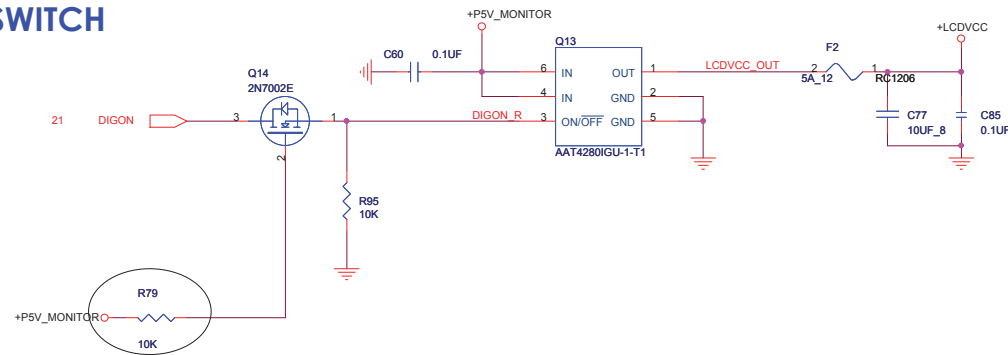
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PROJECT : QU8

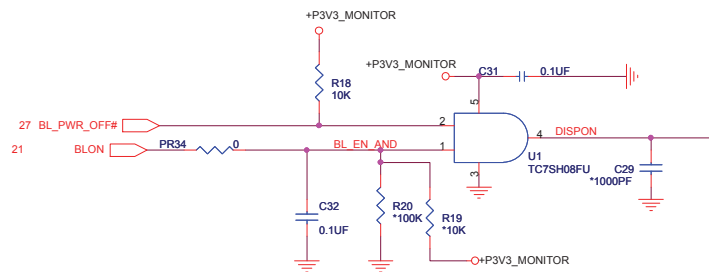
Size	Document Number	Rev
	PCH-GND	D
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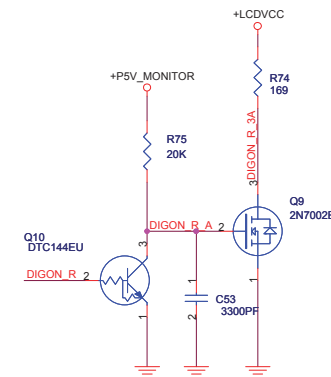
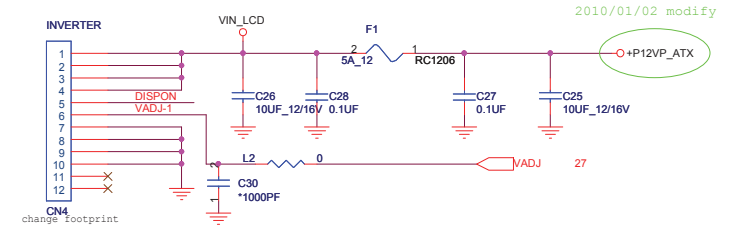
LCD POWER SWITCH



BACKLIGHT CONTROL



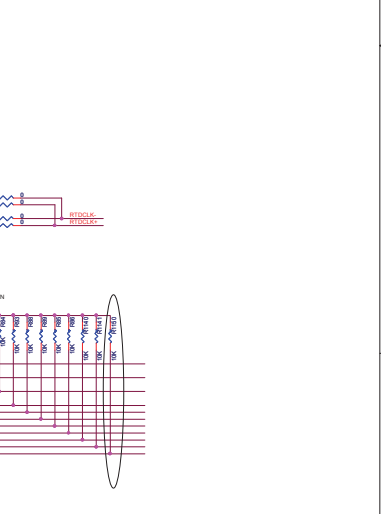
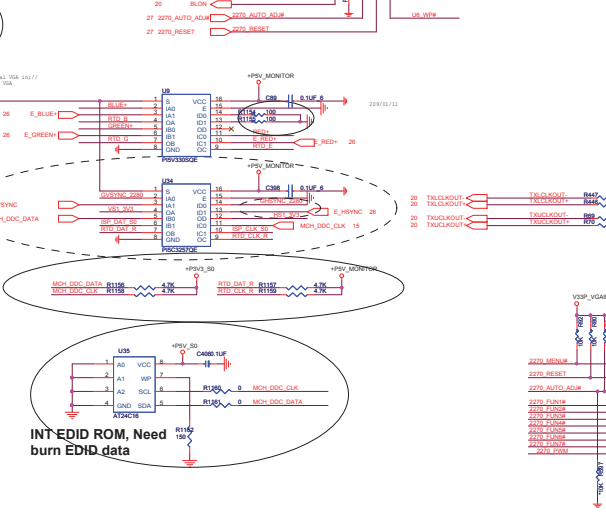
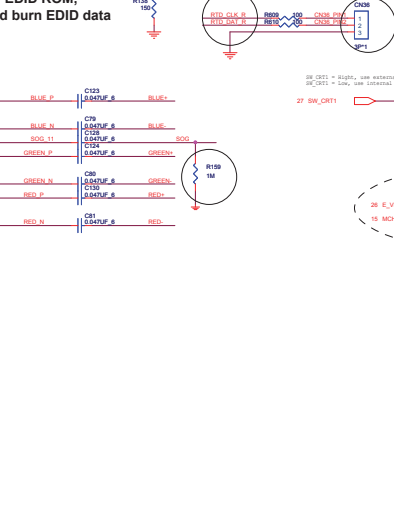
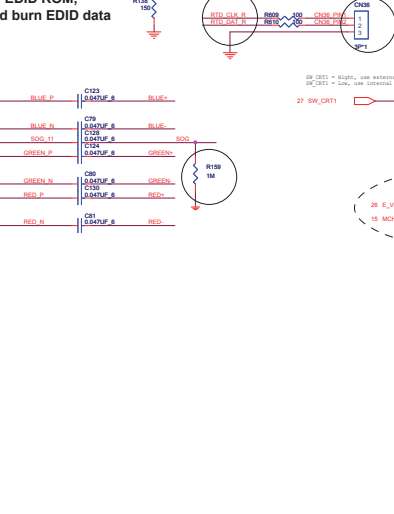
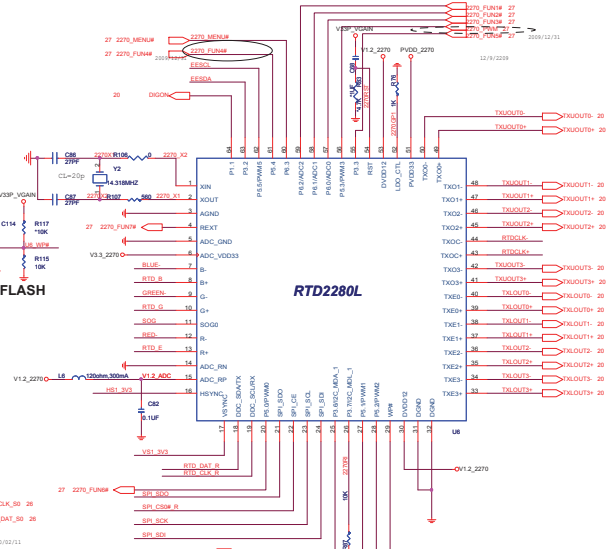
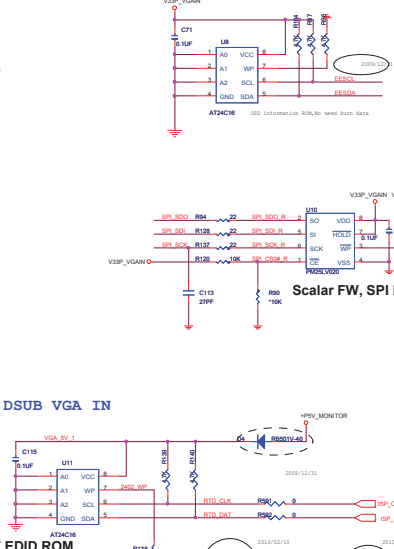
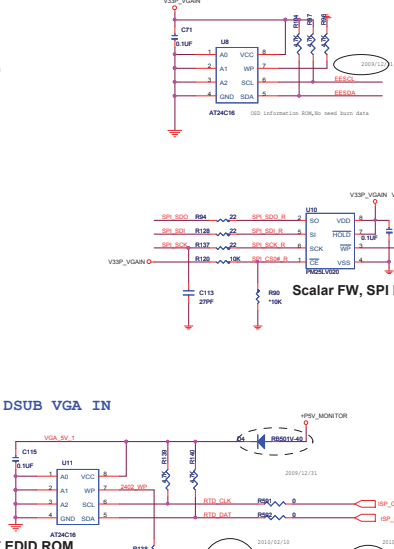
TO INVERTER POWER



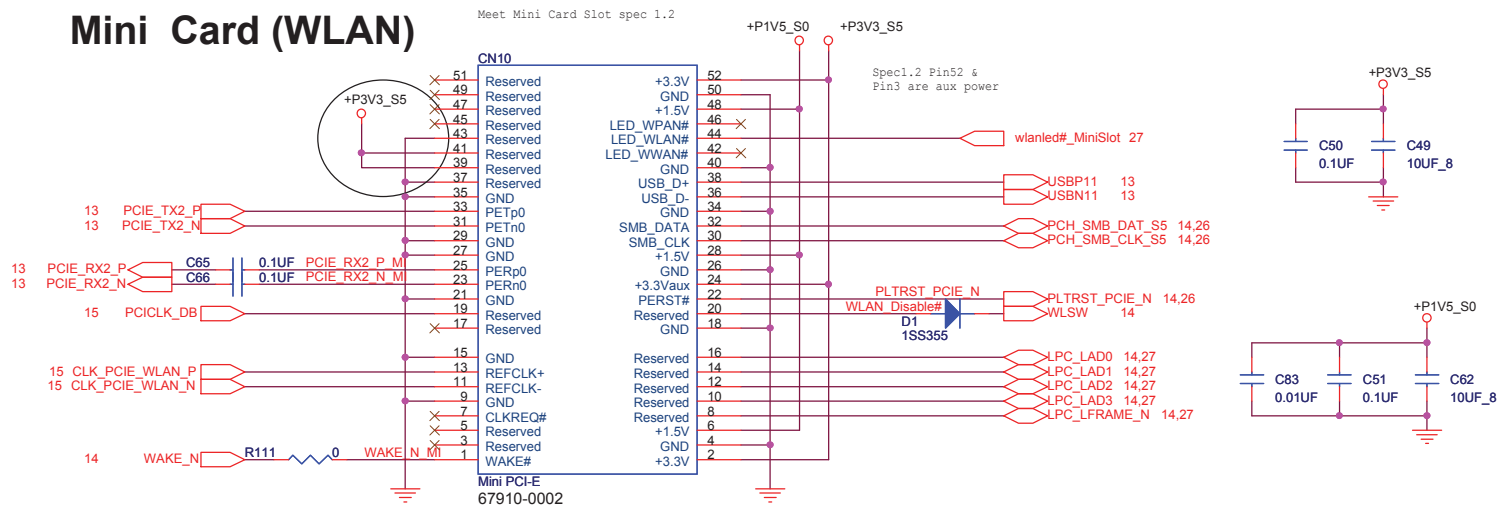
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PROJECT : Q08

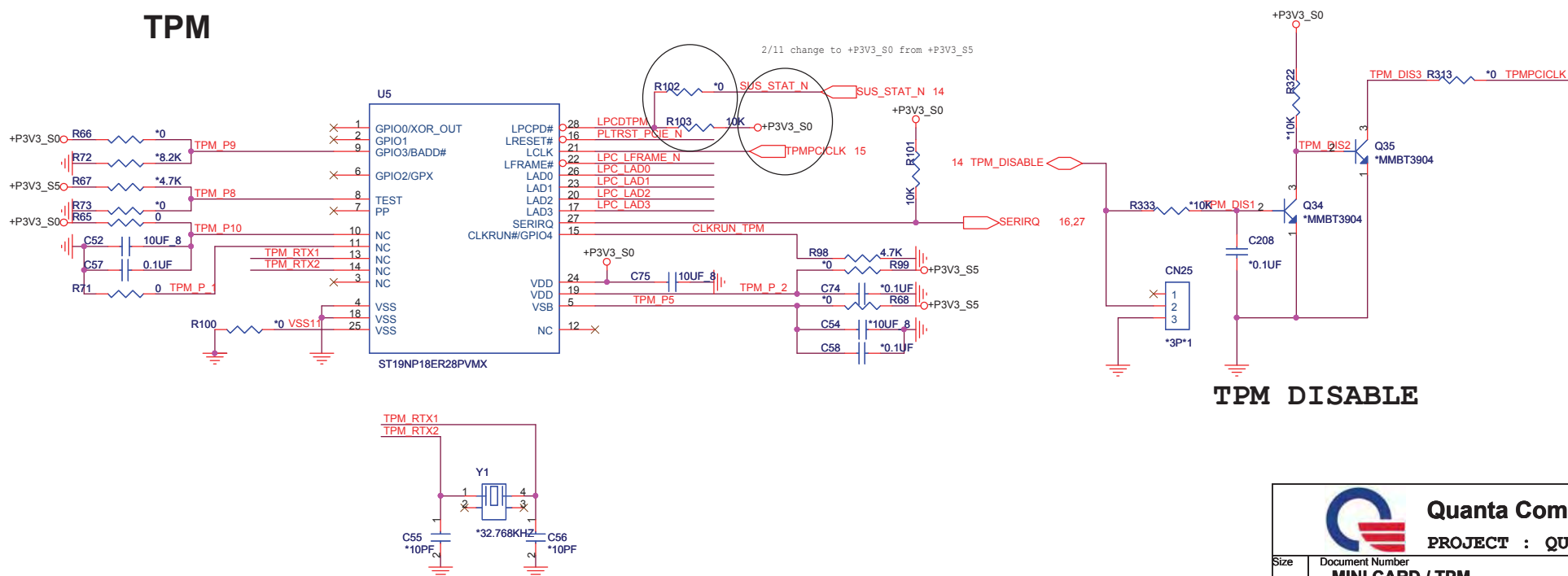
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	LCD/INVERTER	
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Mini Card (WLAN)



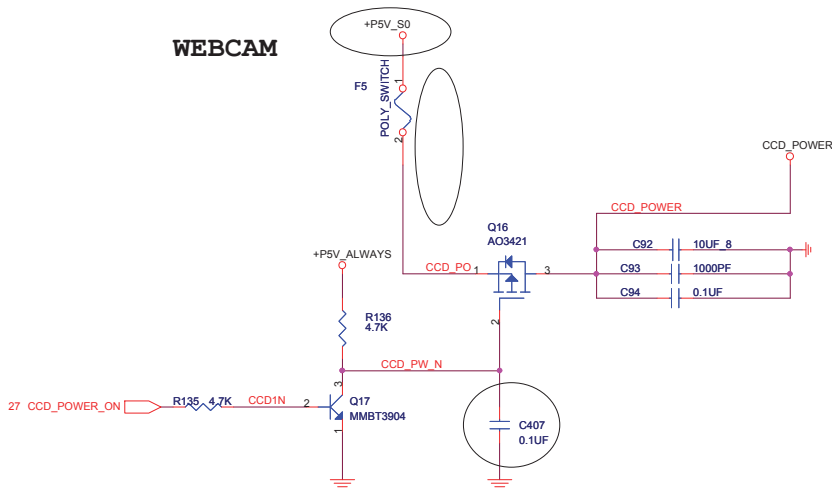
TPM



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PROJECT : QU8

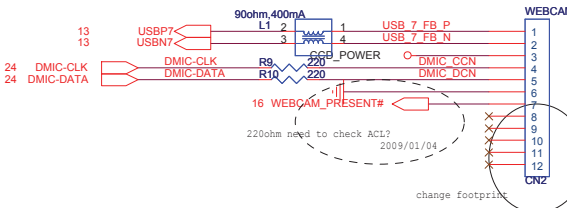
Size	Document Number MINI CARD / TPM		
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WEBCAM

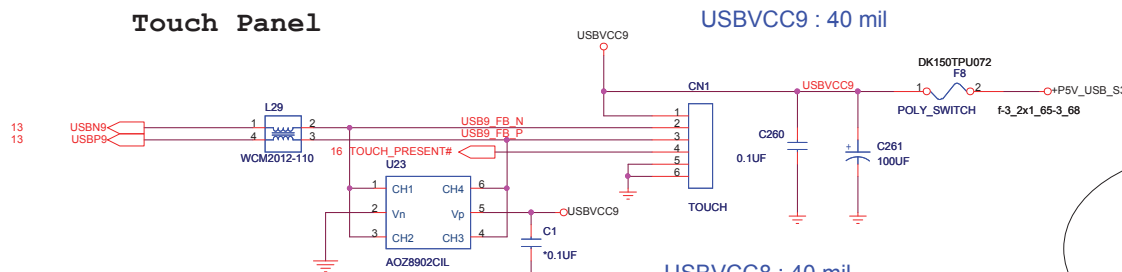


WEB CAM MODULE

FOR EMI

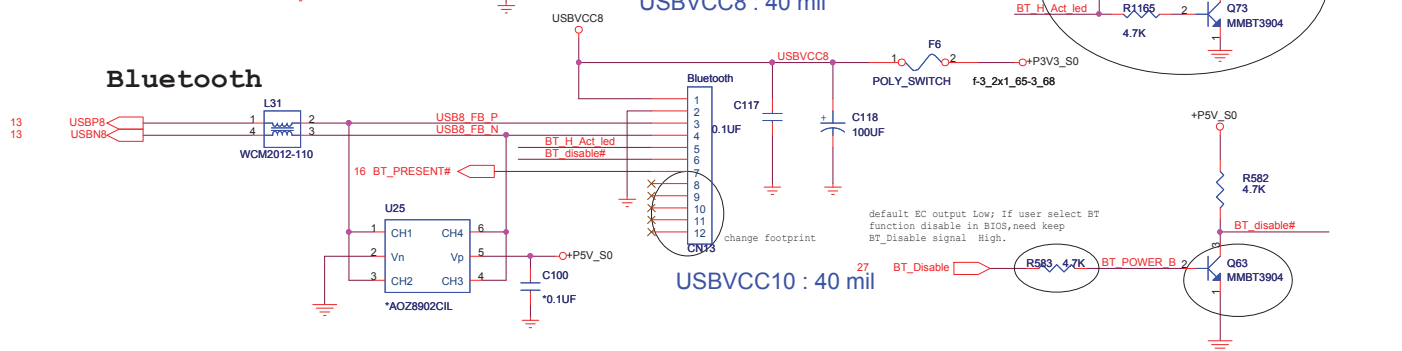


Touch Panel



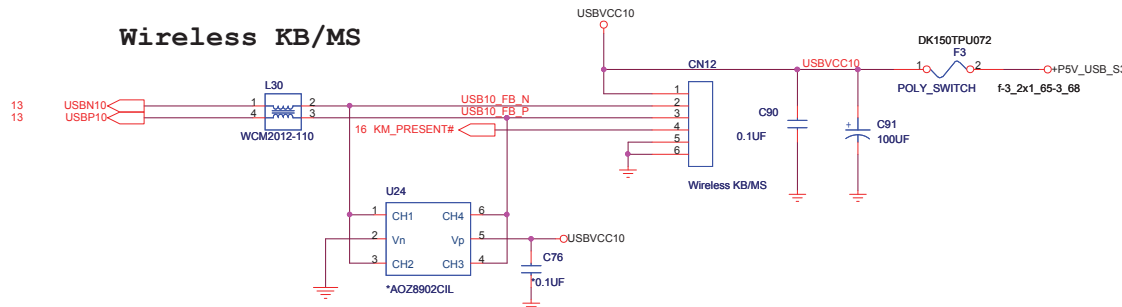
USBVCC8 : 40 mil

Bluetooth



USBVCC10 : 40 mil

Wireless KB/MS

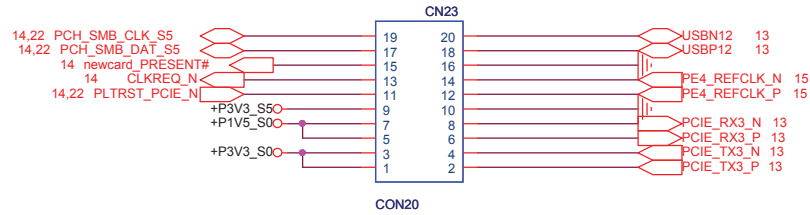


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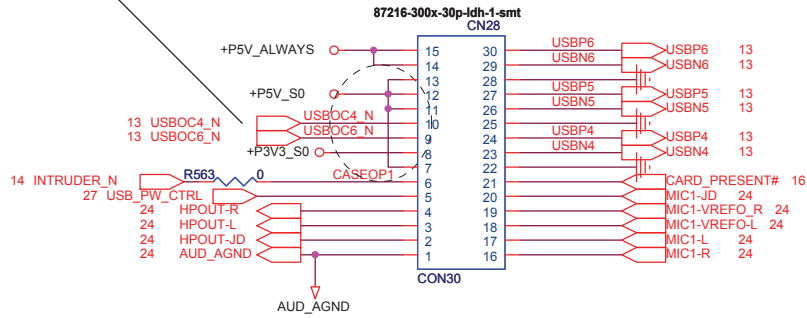
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Size	Document Number	Rev
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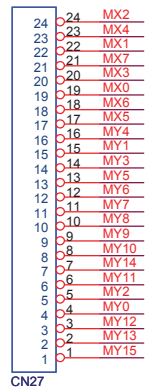
New Card Board



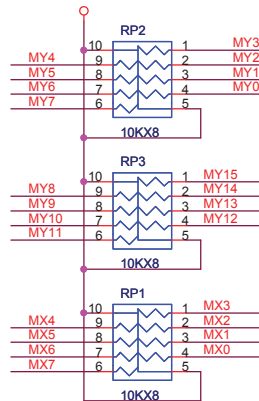
Right IO Board 2 X15



*88502-2401-24P-L

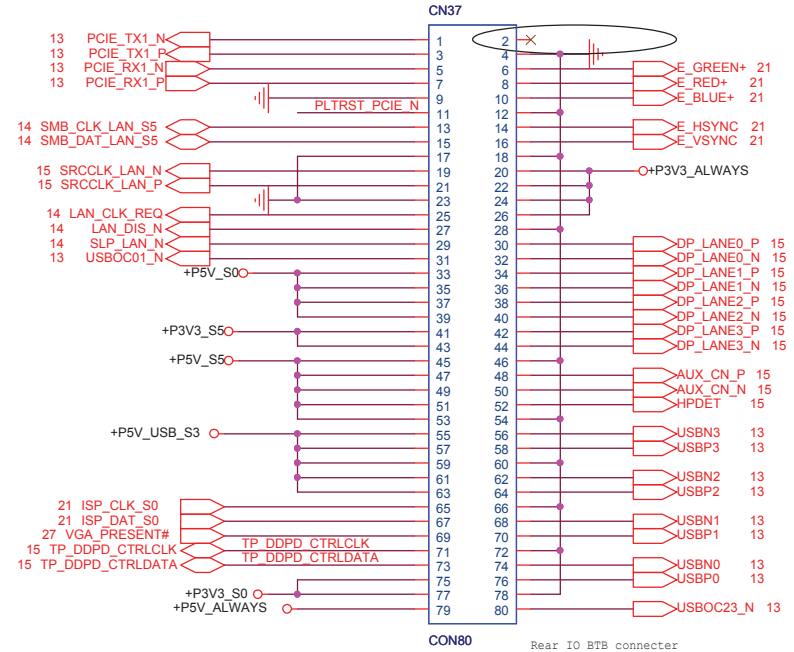


+P3V3_ALWAYS



27 MY[7..0]
27 MY[15..0]

2/23/2010
Del +VCC1_8_PCH_S0



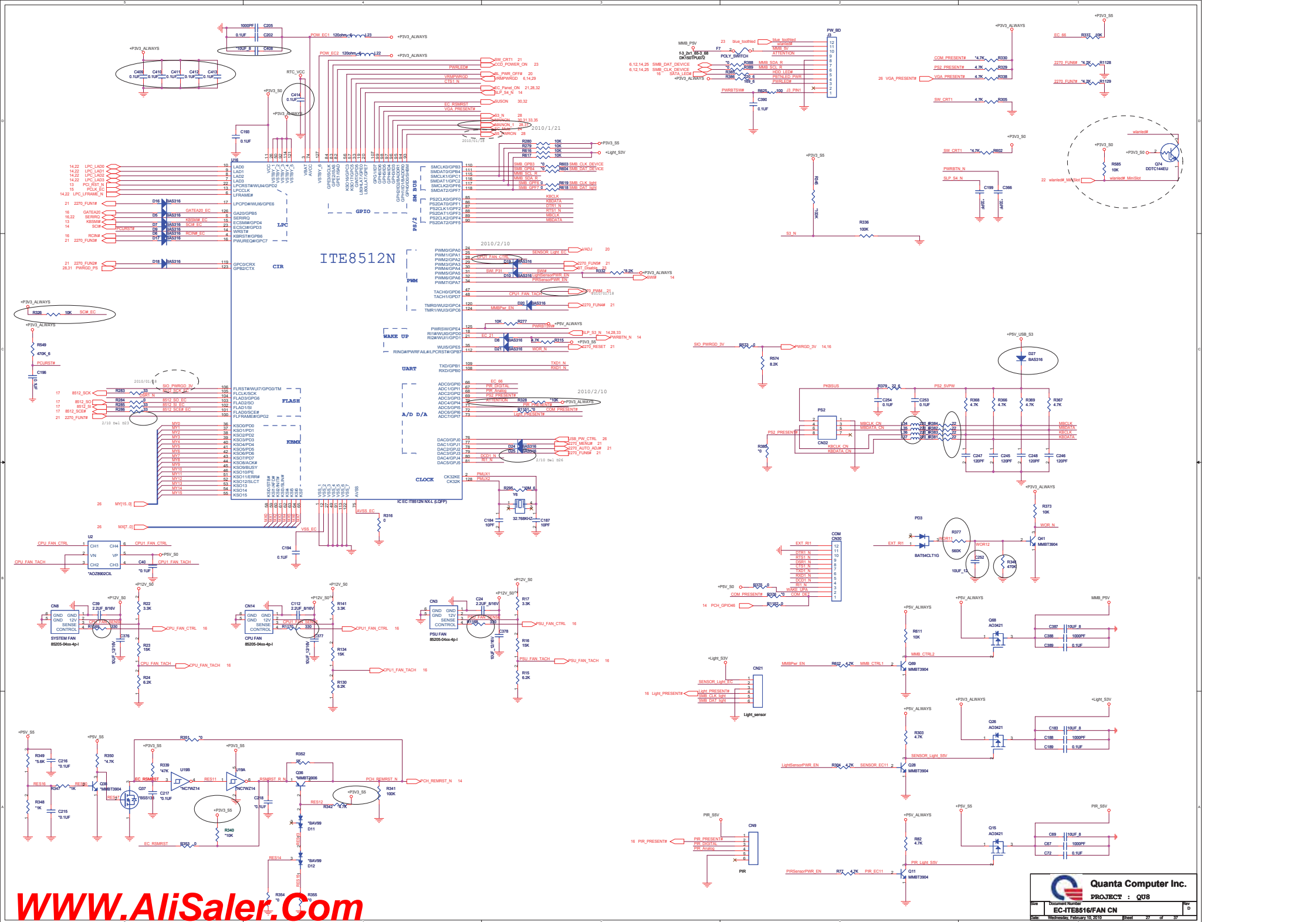
Rear IO BTB connector



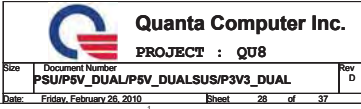
Quanta Computer Inc.

PROJECT : QU8

Size	Document Number	Rev
	27-Daughter Board	D
Date:	Tuesday, February 23, 2010	Sheet 26 of 37



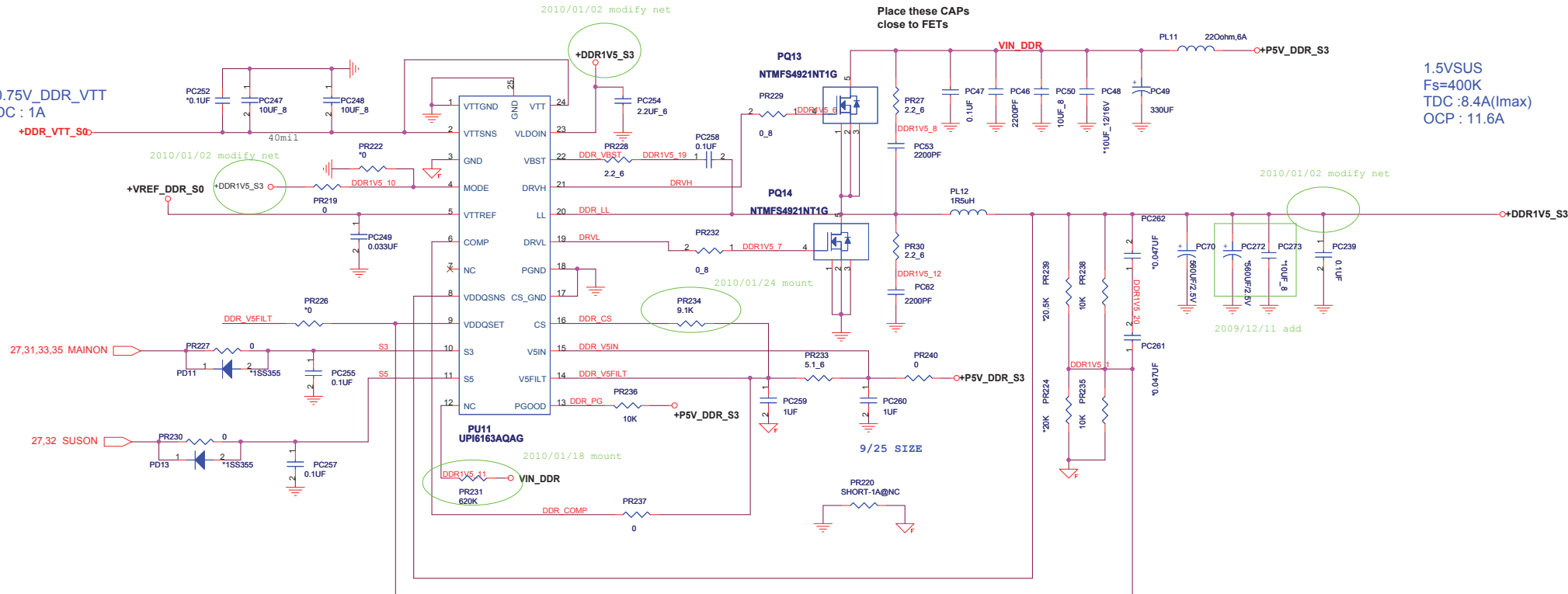
PJ1
PWR CON 2X12

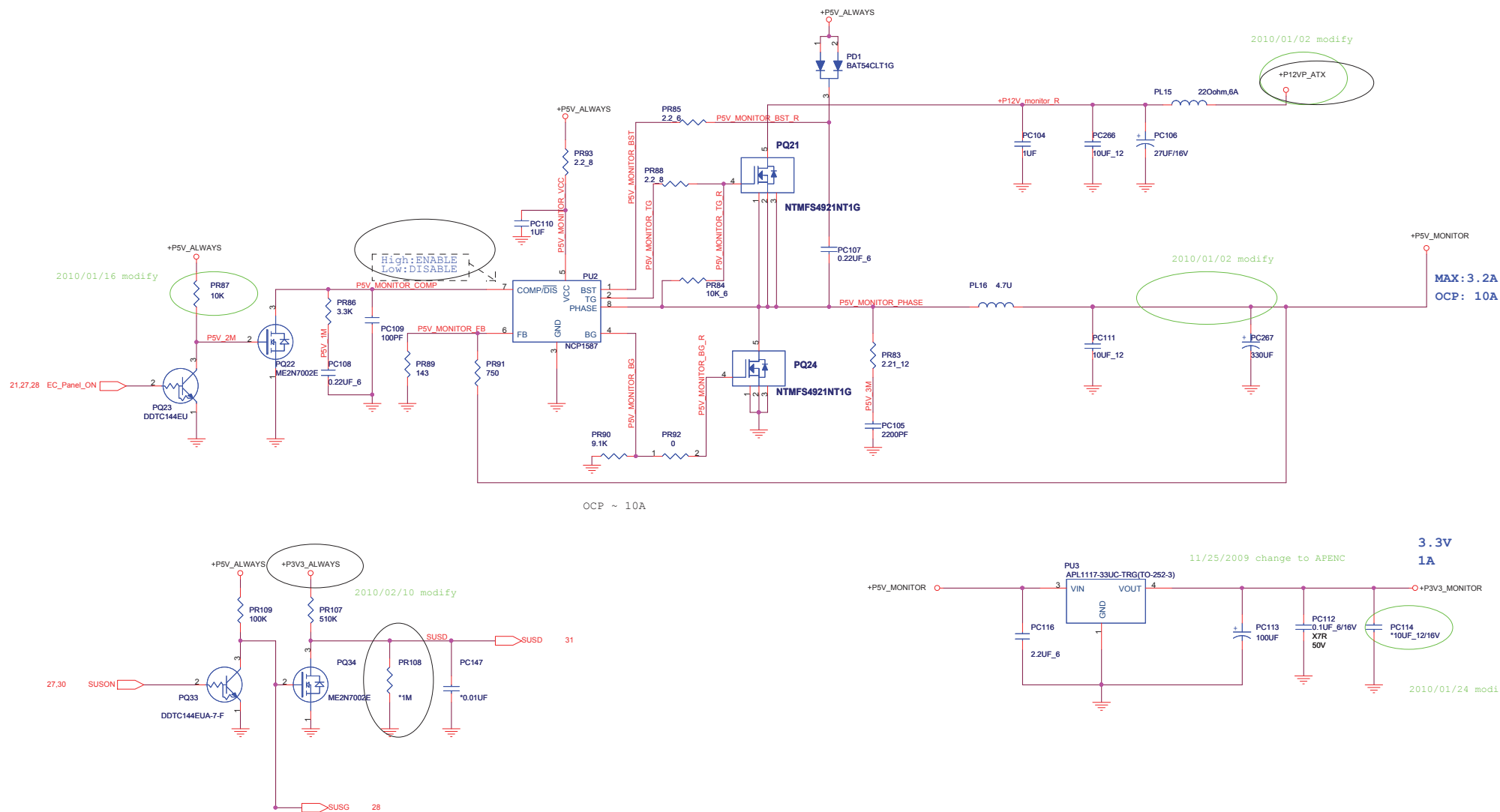


+0.75V_DDR_VTT
TDC : 1A

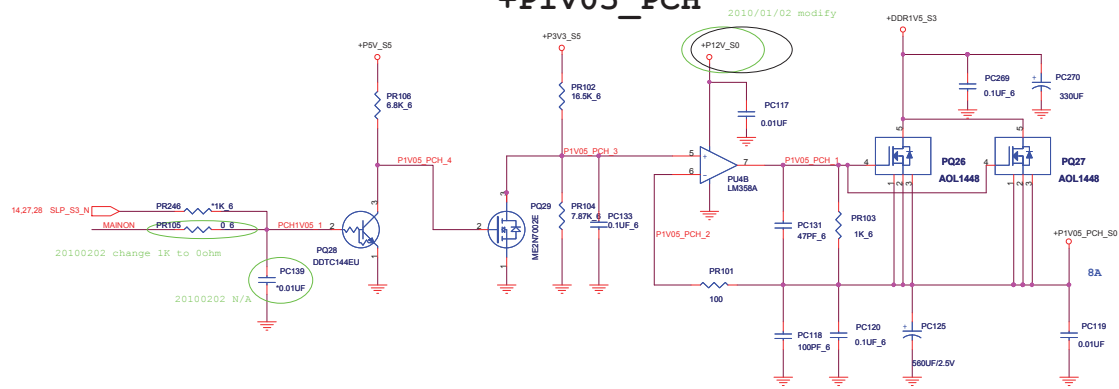
Place these CAPs
close to FETs

1.5VSUS
Fs=400K
TDC :8.4A(I_{max})
OCP : 11.6A

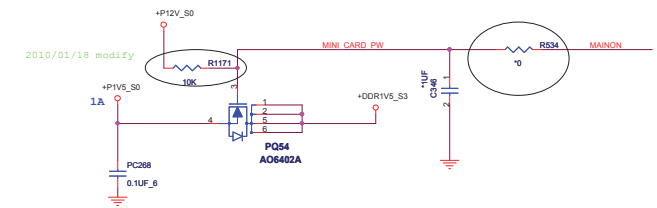




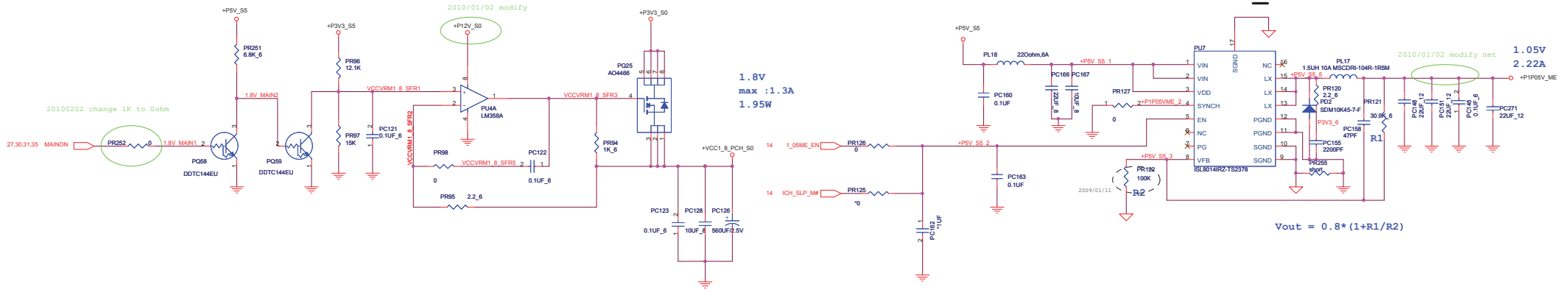
+P1V05 PCH



MINI CARD POWER



+P1P05V_ME

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Size	Document Number
	1P2V/P1V8/P1V05

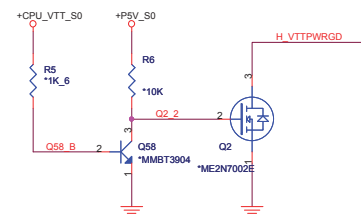
Date: Wednesday, February 24, 2010 Sheet 33 of 37

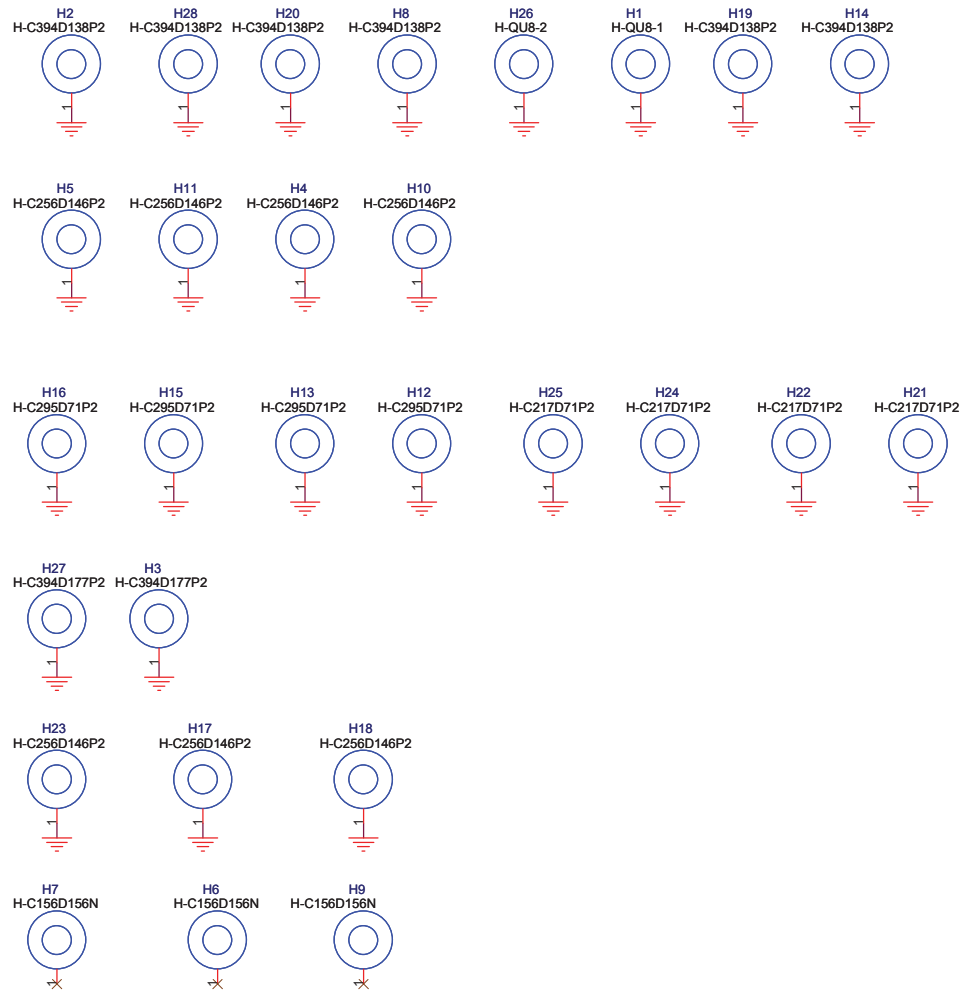
2010/01/02 modify



2009/12/11 change

```
FROM CPU
PIN AE35
```





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Size	Document Number	Rev
	SCREW HOLD, M/E	D
Date: Tuesday, February 23, 2010	Sheet 36 of 37	

NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
PCH_GPIO0	GPIO0	I		INITIAL : HIGH / ACTIVE : LOW
CPU1_FAN_TACH	GPIO1	B	CPU FAN	
PCI_FIRQ#	GPIO2	I	pull up 8.2K to +VDD_30	
PCI__PIRQF#	GPIO3	I	pull up 8.2K to +VDD_30	
PCI_FIRQG#	GPIO4	O	pull up 8.2K to +VDD_30	
PCI_FIRQH#	GPIO5	O	pull up 8.2K to +VDD_30	
PSU_FAN_TACH	GPIO6	I	PSU FAN	
WP#	GPIO7	O	SEC ROM write protect	
PCH_GPIO8	GPIO8	O		
USB0C1011_N	GPIO9	O	USB Over current	
USB0C1213_N	GPIO10	O	USB Over current	
PCH_SMBALERT_N	GPIO11	I	pull up 2.2K to +VDD_35	
LAN_DIS_N	GPIO12	O	0 = GPIO12 default is General Purpose (GP) output 1 = GPIO12 is used to receive wake up LAN000000	
SCI#	GPIO13	O	IC TO PCN ,Interrupts for power management events.	
USB0C1415_N	GPIO14	O	USB Over current	
TLS	GPIO15	O	Confidentiality Higher Privilege (EL2) higher state with no confidentiality High -EL2 higher state with confidentiality	
GPIO16	GPIO16	I	pull up 10K to +VDD_35	
CPU_FAN_TACH	GPIO17	I	CPU Fan Tachometer Input	
WLSW	GPIO18	I	WLAN(WLAN_FCTN) SW	
VGA_PRESENT	GPIO19	I	Serial ATA 1 General Purpose	
CLKREQ_N	GPIO20	I	New card to PCN	
CARD_PRESENT	GPIO21	I	Serial ATA 0 General Purpose	
TOUCH_PRESENT	GPIO22	I	pull up 10K to +VDD	
TP_PCH_GPIO23	GPIO23	I		
SPI_WP_N	GPIO24	O		
SWI#	GPIO25	O	pull up 8.2K to +VDD_35	
SPI_WP_SMI	GPIO26	O	pull up 8.2K to +VDD_35	
PCH_GPIO27	GPIO27	I	enable/disable PLL VR	
PCH_GPIO28	GPIO28	I	GPIO28 is multiplexed with SPI_SMI functionality, which may be utilized only for module configurations	
SLP_LAN_N	GPIO29		When SLP_LAN is deactivated it indicates that the Networked HW device must be powered. (pull up 8.2K to +VDD_35, 0V)	
SUS_PWR_ACK	GPIO30		pull up 100K to +VDD_35	
PCH_BLOCK_RESET_N	GPIO31		pull up 8.2K to +VDD_35	
newcard_PRESENT	GPIO32		Test point	
PCH_GPIO33	GPIO33		connect to CN2 (Reserved)	
STP_PCI_N	GPIO34		pull up 8.2K to +VDD_30	
SATACLKREQ_N	GPIO35		pull up 8.2K to +VDD_35	

NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
LIGHT_PRESENT	GPIO36	I	Serial ATA 2 General Purpose	
FIR_PRESENT	GPIO37	B	Serial ATA 3 General Purpose	
WEBCAM_PRESENT	GPIO38	I	Webcam detect	
BT_PRESENT	GPIO39	I	Bluetooth detect	
USB0C23_N	GPIO40	O	USB Over current	
USB0C4_N	GPIO41	O	USB Over current	
USB0C6_N	GPIO42	I	USB Over current	
USB0C89_N	GPIO43	O	USB Over current	
LAN_CLK_REQ	GPIO44	O	Clock Request Signal for PCI Express. PCN to Back IO	
PCH_GPIO45	GPIO45	O	connect to CN13 (Clear CMOS or normal)	
PD_SRC7CLKREQ_N	GPIO46	O	pull up 8.2K to +VDD_35	
PD_FEG_A_CLKREQ_N	GPIO47	I	Clock Request Signal for PS0 SLOTS	
KM_PRESENT	GPIO48	O	Wireless LAN detect	
KBSMI#	GPIO49	O	IC to PCN	
PCI_REQ1#	GPIO50	O	pull up 8.2K to +VDD_30	
PCI32_GNT_N1	GPIO51	O		
PCI_REQ2#	GPIO52	I	pull up 8.2K to +VDD_30	
ESI_STRAP	GPIO53	I		
PCI_REQ3#	GPIO54	I	pull up 8.2K to +VDD_30	
PCI32_GNT_N3	GPIO55	I		
TPM_DISABLE	GPIO56	I	pull up 8.2K to +VDD_35	
PCH_GPIO57	GPIO57	I	pull low 10K to GND	
SMB_LINK1_CLK	GPIO58	I	SMbus_CLK (F5174)	
USB0C01_N	GPIO59	I	USB Over current	
SMB_ALERT#	GPIO60	O	pull up 10K to +VDD_35	
SUS_STAT_N	GPIO61	O	pull up 8.2K to +VDD_35 (Hi)	
SUSCLK	GPIO62	O	pull up 8.2K to +VDD_30at	
FM_SLP35_N	GPIO63	I	Test point (F5176)	
PCH_AD10	GPIO64	I		
PCH_AK1	GPIO65			
PCH_AB6	GPIO66			
PCH_AL3	GPIO67			
GPIO72	GPIO72		pull up 8.2K to +VDD_35	
PCH_GPIO73	GPIO73		pull up 10K to +VDD_30	
PCH_AY32	GPIO74		pull up 10K to +VDD_35	
SMB_LINK1_DAT	GPIO75		SMbus_DATA (F5175)	